UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,863	10/25/2001	Donald Thomas McGrath	RD-27645	9978

23465 7590 04/09/2003

JOHN S. BEULICK
C/O ARMSTRONG TEASDALE, LLP
ONE METROPOLITAN SQUARE
SUITE 2600
ST LOUIS, MO 63102-2740

EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-682,863	McGrath
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 3-24-2003.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-24 ☒/are pending in the application.

Of the above claim(s) 6-9 ☒/are withdrawn from consideration.

☒ Claim(s) 10-21 ☒/are allowed.

☒ Claim(s) 1-4, 22 and 23 ☒/are rejected.

☒ Claim(s) 5 and 24 ☒/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as set forth on page 6, paragraph labeled "[0018]" (AAPA) in view of Palmour et al. "High-temperature depletion-mode metal-oxide-semiconductor field-effect transistors in beta-SiC thin films" Appl. Phys. Lett. 51, 14 December 1987 pp2028-2030 (Palmour) and Slater, Jr. et al. US 6,344,663 (Slater).

AAPA states: "[0018] Referring to Figure 4, the remaining circuitry of chopper stabilized NMOS depletion mode operational amplifier 10 are **conventional**. In the topology shown in Figure 4, chopping switch 18 has threshold voltages that are negative with respect to the drains and sources of (and thus, the channels of) FETs Q7, Q8, Q9, and Q10. Similarly, chopping switch 20 has threshold voltages that are negative with respect to the drains and sources of FETs Q11 , Q12, Q13, and Q14. Differences in source potentials for switches 18 and 20 require level shifting of drive voltages applied to the gates of their respective FETs to turn the switches on and off. This level shifting is provided by BFL level shifting circuits 28 and 30 (not shown in Figure 4). The use of either circuit 44 or 64 as a BFL level shifting circuit allows an inverter to drive both sets of chopping switches simultaneously without the use of additional level shifting circuitry. Offsets in amplifier 10 are removed dynamically so that offset drift and flicker noise are substantially reduced or minimized.(emphasis added)" Therefore, the circuit shown by Figure 4 is conventional, however, applicant forms an embodiment that is "implemented in NMOS depletion mode silicon carbide (SiC) technology".

The functioning of the AAPA circuit results in a method for amplifying a signal having the steps of generating an input signal INN, INP from an outside source, and amplifying this input signal utilizing a chopper-stabilized 18, 20, NMOS depletion mode operational amplifier 22, 24 to produce an amplified

output signal OUT, the operational amplifier including a first NMOS depiction mode amplification stage 22 and a second NMOS depletion mode amplification stage 24. The functioning of the AAPA circuit additionally results in the further steps of chopping the input signal utilizing a first NMOS depletion mode chopping switch 18 responsive to a first level shifted chopping signal 32, 36 to produce a first chopped input signal CNA, CNB. The functioning of the AAPA circuit additionally results in the further steps of amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage 22 to produce an amplified chopped output signal 40, 42. The functioning of the AAPA circuit additionally results in the further steps of chopping the amplified chopped output signal 40, 42 utilizing an NMOS depletion mode amplifier 24, the NMOS depletion mode amplifier 24 being responsive to a level shifted first chopping signal 32, 36 to produce a chopper-stabilized output signal CNA, CNB. AAPA is silent on the NMOS transistors being formed from SiC or any other material. AAPA only generically shows NMOS transistors for the choppers and operational amplifier elements. AAPA is also silent on the forming of the first and second stage on the same substrate.

Palmour discloses one conventional form of NMOS depletion mode transistors, namely the NMOS depletion mode transistors formed from SiC (See Figure 1). Palmour also discloses advantages of deploying such transistors such as the allowance of high temperature operation, the good high frequency characteristics and the ability of being able to operate at high power (See the first paragraph on page 2028 of Palmour).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional NMOS depletion mode transistors formed from SiC in place of the generic transistors of AAPA because, as AAPA is silent on the material forming these NMOS depletion mode transistors, any art-recognized material would have been usable such as the well-known, conventional SiC material as disclosed by Palmour. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional NMOS depletion mode transistors formed from SiC in place of the generic transistors of AAPA so as to allow for high temperature, high power and high frequency operation as taught by Palmour.

Slater discloses forming of at least two SiC MOSFET transistors on a single substrate (See Figure 2). This is commonly called integration and it is well known that this saves space in the forming of a circuit over the forming of a circuit using discrete elements.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the step of forming the invention made obvious above on the same silicon carbide substrate as taught by Slater.

Allowable Subject Matter

Claims 10-21 are allowed.

The prior art or record fails to disclose or suggest the combination of a chopper/amplifier/chopper/amplifier structure and an NMOS depletion mode buffered field effect transistor logic (BFL) wherein the NMOS depletion buffered field effect transistor logic (BFL) is taken to mean an BFL circuit with just NMOS depletion mode field elect transistors as the main components thereof as reflected in the interview held 1-16-2003 and the remarks of 3-24-2003.

Claims 5 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims are allowable for the same reasons that claims 10-21 are allowable.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schmid et al. "Process Technology and High Temperature Performance of 6H-SiC MOS Devices" discloses that SiC devices are ideal for forming circuits used in high temperature environments such as combustion and exhaust gas monitoring, oil-drilling, aerospace, automotive and nuclear industries. Onishi et al. JP 58,130,608 discloses the general state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
April 3, 2002

Michael B Shingleton

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817